

1. The present invention relates to a method of manufacturing a semiconductor device, and more particularly to a method of manufacturing a semiconductor device having a central opening.

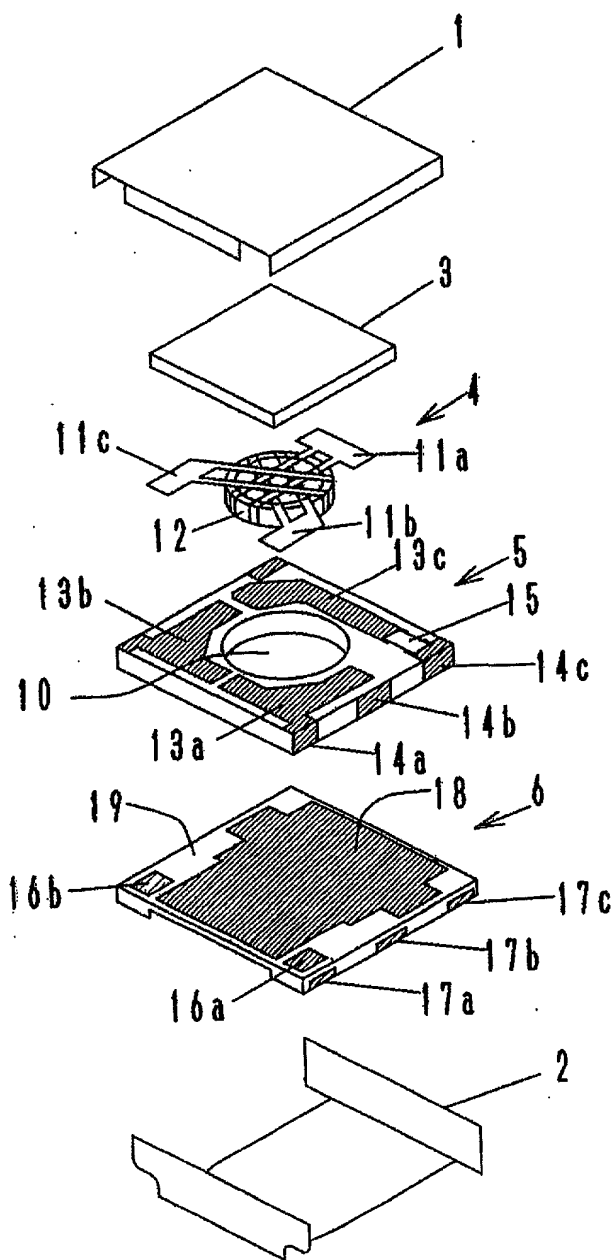


Fig. 1

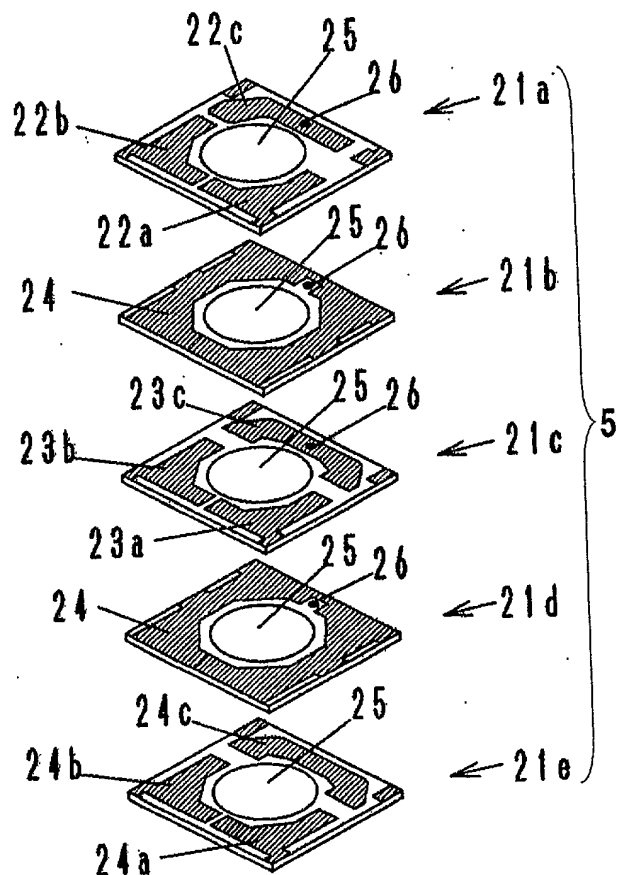


Fig. 2

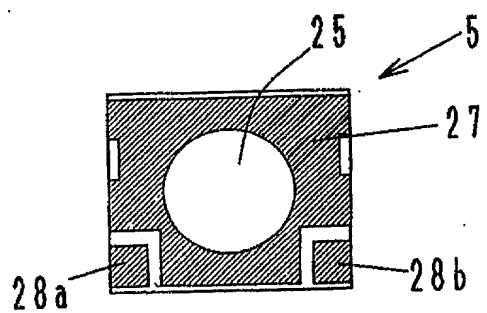


Fig. 3

Fig. 4

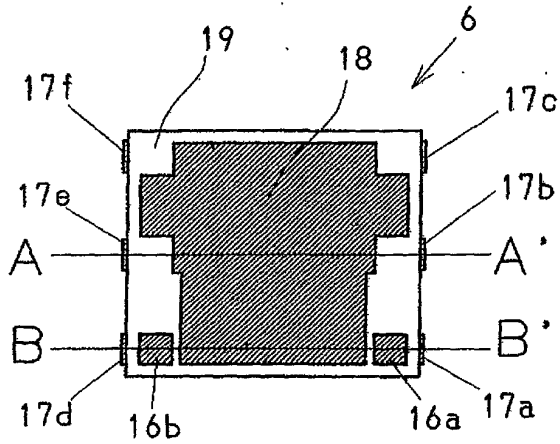


Fig. 5



Fig. 6

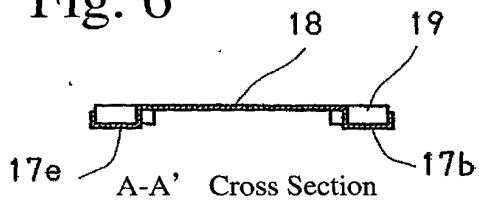


Fig. 7

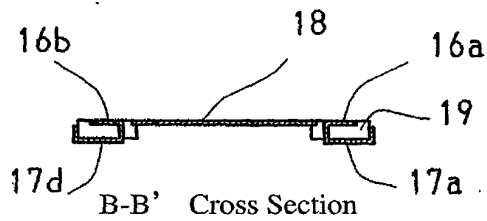


Fig. 8

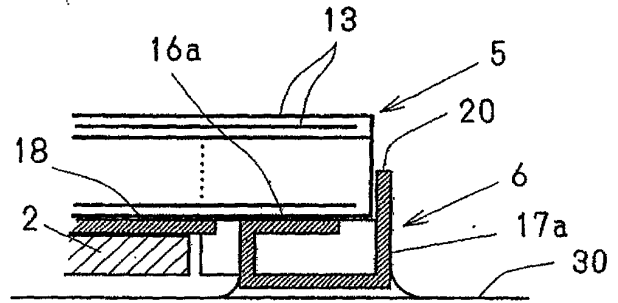


Fig. 11(a)

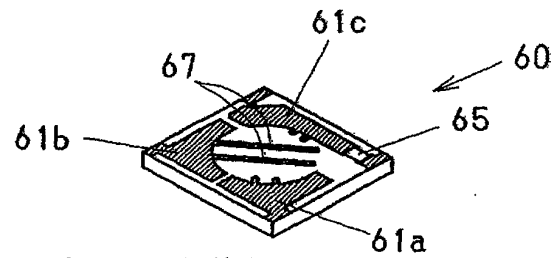


Fig. 11(b)

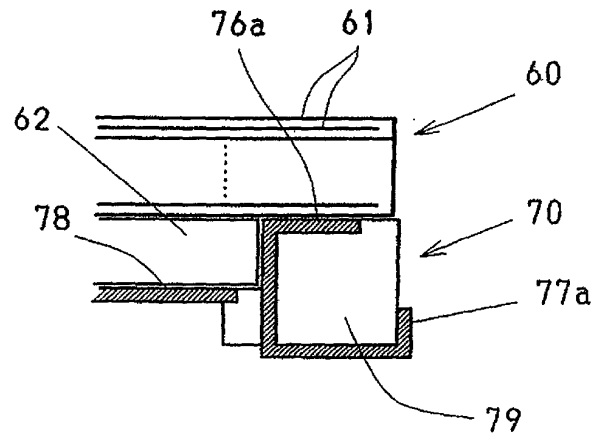


FIG. 9 is a perspective view of a first embodiment of a device 100. The device 100 includes a top plate 1, a middle plate 3, and a bottom plate 2. A central component 40 is positioned between the middle plate 3 and the bottom plate 2. The central component 40 includes a central square region 41a, four side regions 41b, 41c, 41d, and 41e, and four corner regions 42. A central square region 45 is also shown. The central component 40 is connected to a central square region 50, which is further connected to a central square region 55. The central square region 55 is connected to a central square region 57. The central square region 57 is connected to a central square region 51a, 51b, 51c, and 51d. The central square region 51a is connected to a central square region 52a, 52b, 52c, and 52d. The central square region 52a is connected to a central square region 16a, 16b, 16c, and 16d. The central square region 16a is connected to a central square region 17a, 17b, 17c, and 17d. The central square region 17a is connected to a central square region 18. The central square region 18 is connected to a central square region 2. The central square region 2 is connected to a central square region 100.

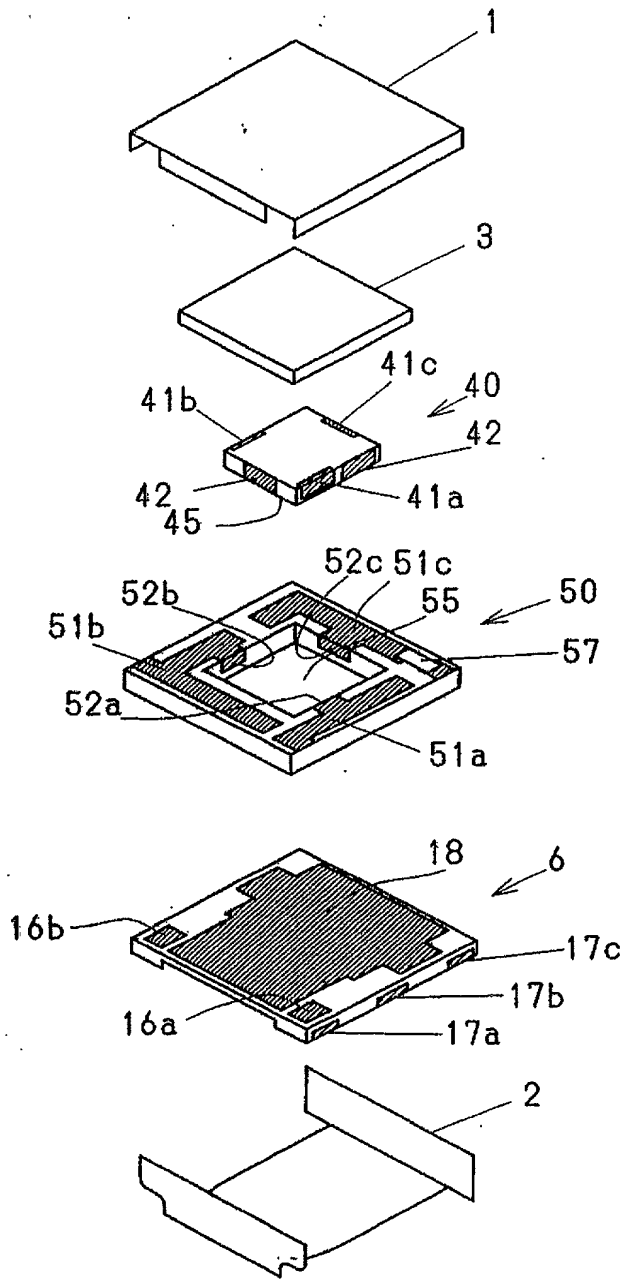


Fig. 9

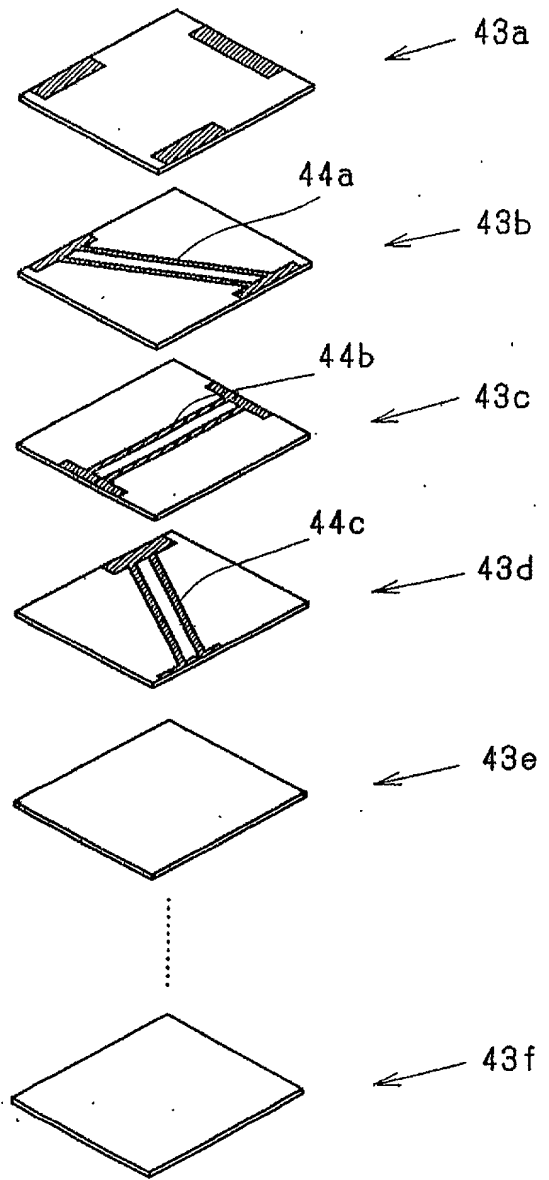


Fig. 10

Fig. 12

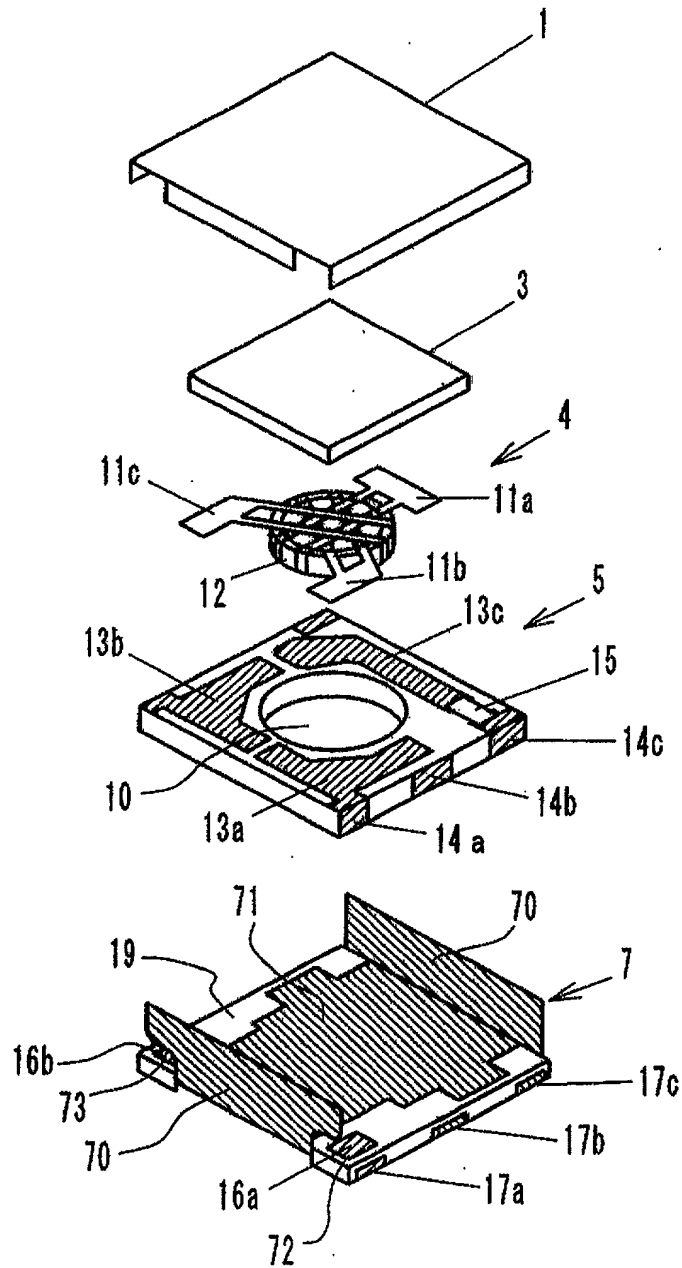


Fig. 13

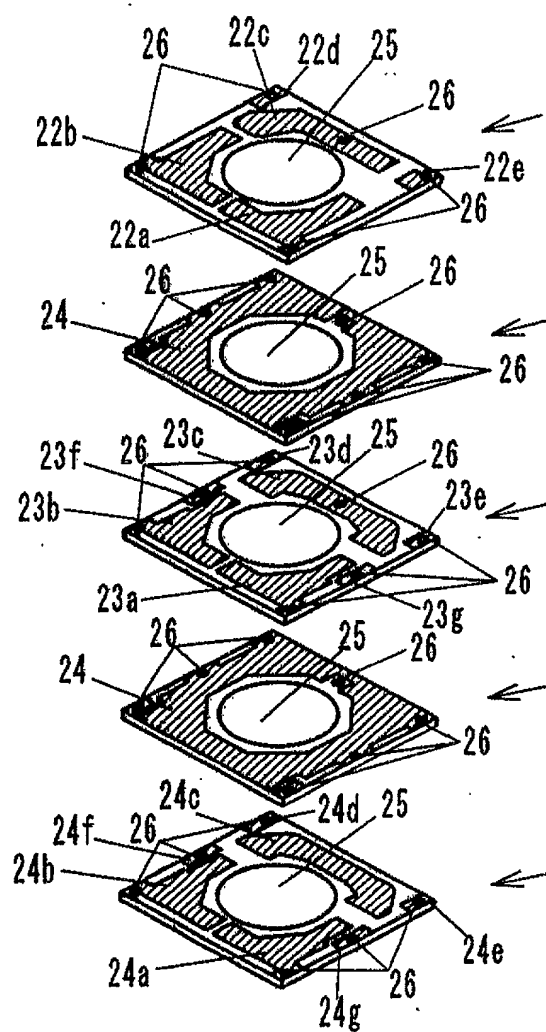


Fig. 14

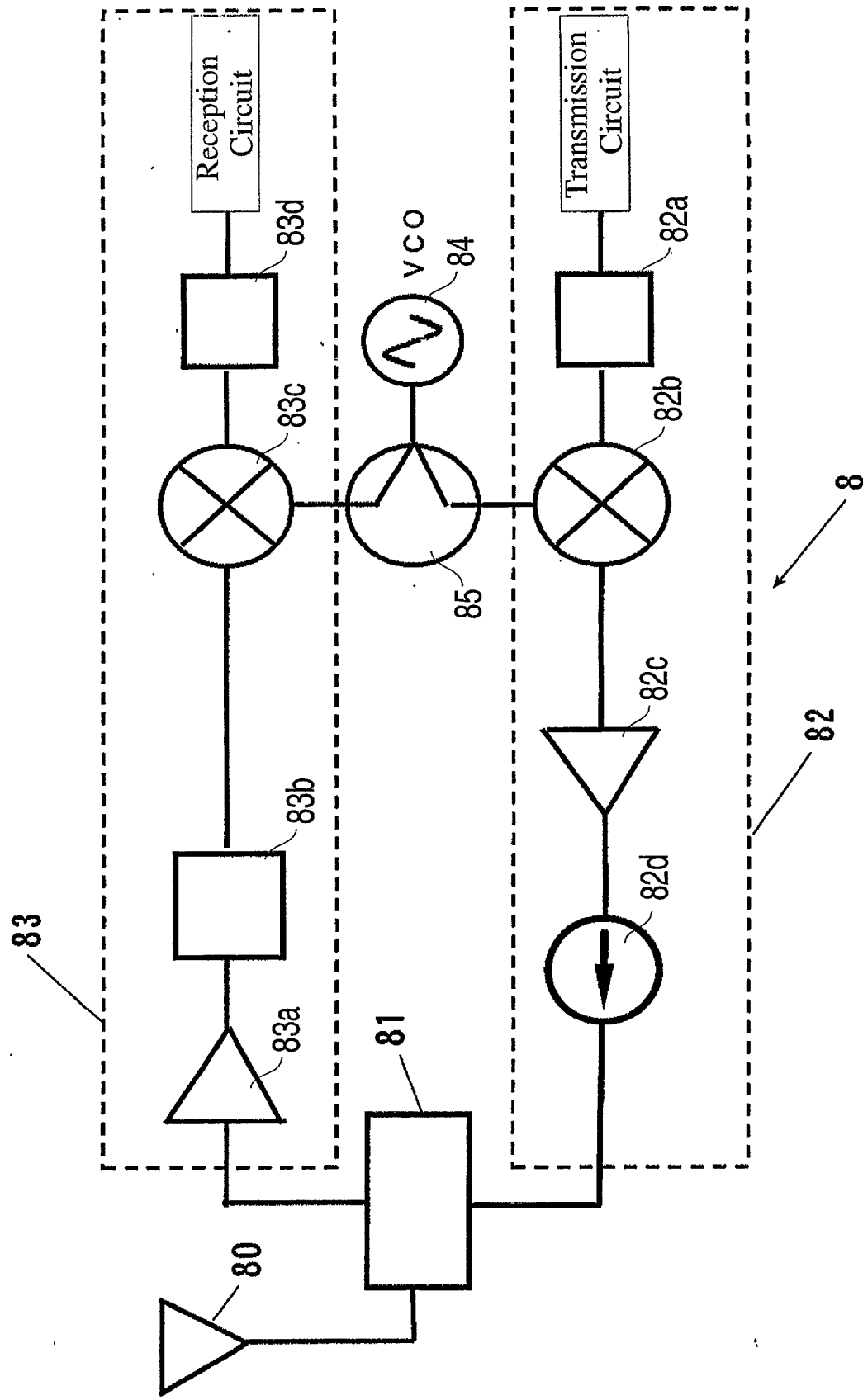


Fig. 15

PRIOR ART

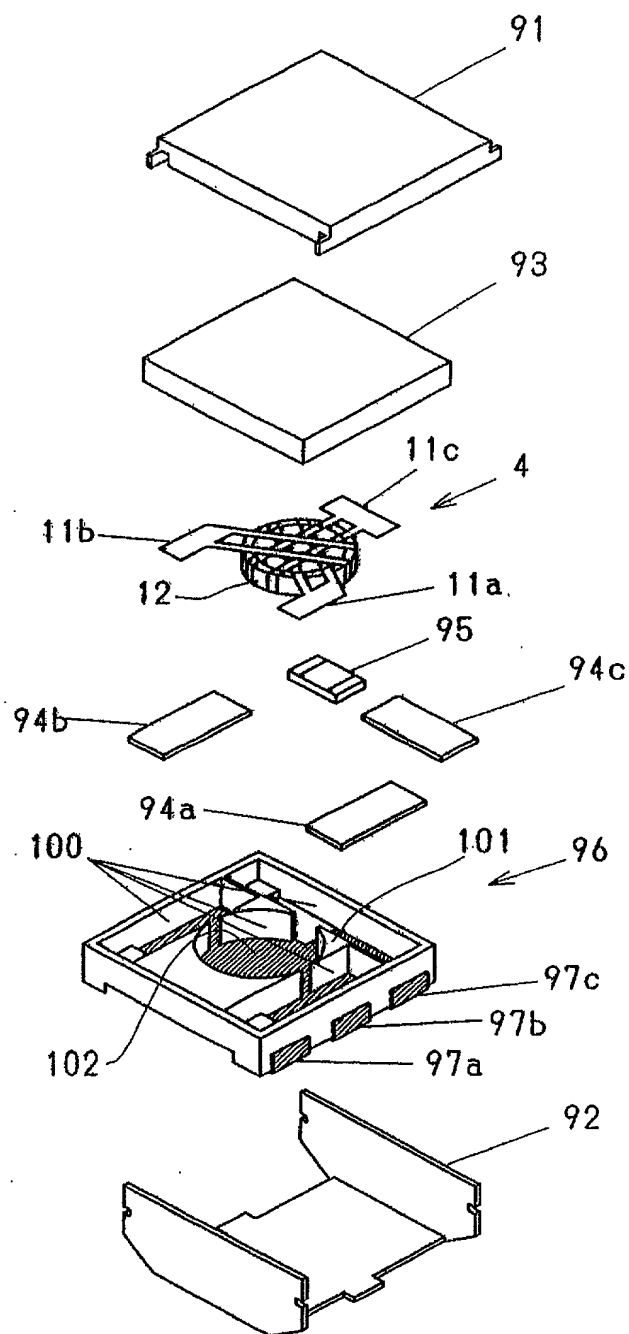


Fig. 16

PRIOR ART

